Form PTO-1449 (modified) List of Patents and Publications For Applicant's Information Disclosure Statement (Use several sheets if necessary)	ATTY. DKT. NO. 5580-04900 APPLICANT: Santhanam, et al. FILING DATE: February 1, 2002	SERIAL NO. 10/061,695 GROUP: 2182

U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
AW	B1	6,535,036	3/18/03	Dobberpuhl			

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER: A Wang DATE CONSIDERED: 12-20-04

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

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EXAM. INITIALS	REF. DES.	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB	FILING DATE IF APPROPRIATE
aw	A13	5,459,736	10/17/95	Nakamura			
aw	A14	5,689,517	11/18/97	Ruparel			
aw	A15	6,318,911	11/20/01	Kitahara			
aw	A16	6,247,134	6/12/01	Sproch, et al.			
aw	A17	6,272,667	8/7/01	Minami, et al.			
aw	A18	5,815,725	9/29/98	Feierbach			
aw	A19	4,061,933	12/6/77	Schroeder, et al.			
aw	A20	5,831,462	11/3/98	Witt, et al.			
aw	A21	6,223,282	4/24/01	Kang			
aw	A22	6,411,152	6/25/02	Dobberpuhl			

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aw	A1	SiByte, "Target Applications," http://sibyte.com/mercurian/applications.htm, January 15, 2001, 2 pages.
aw	A2	SiByte, "SiByte Technology," http://sibyte.com/mercurian/technology.htm, January 15, 2001, 3 pages.
aw	A3	SiByte, "The Mercurian Processor," http://sibyte.com/mercurian, January 15, 2001, 2 pages.
aw	A4	SiByte, "Fact Sheet," SB-1 CPU, October 2000, rev. 0.1, 1 page.
aw	A5	SiByte, "Fact Sheet," SB-1250, October 2000, rev. 0.2, 10 pages.
aw	A6	Stepanian, SiByte, "SiByte SB-1 MIPS64 CPU Core, Embedded Processor Forum 2000, June 13, 2000, 15 pages.
aw	A7	Jim Keller, "The Mercurian Processor: A High Performance, Power-Efficient CMP for Networking," October 10, 2000, 22 pages.
aw	A8	Tom R. Halfhill, "SiByte Reveals 64-Bit Core For NPUs; Independent MIPS64 Design Combines Low Power, High Performance," Microdesign Resources, June 2000, Microprocessor Report, 4 pages.
aw	A9	SiByte, Letter from Anu Sundaresan, May 18, 2000, 1 page.
aw	A10	Stephany, et al., "FP 15.5: A 200 MHz 32b 0.5W CMOS RISC Microprocessor," Digital Semiconductor, Austin, TX, IEEE, 1998, pages 15.5-1 to 15.5-9.
aw	A11	Santhanam, et al., "SA 18.6: A Low-Cost 300MHz RISC CPU with Attached Media Processor," Digital Equipment Corp., Palo Alto, CA, IEEE, 1998, pages 18.6-1 to 18.6-9.
aw	A12	Montanaro, et al., "A 160-MHz, 32-b, 0.5-W CMOS RISC Microprocessor," IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, 12 pages.

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